Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies (CHIPS)

Daniel S. Green

U.S. Defense Advanced Research Projects Agency (DARPA)

CHIPS Proposers Day
Falls Church, VA

September 21, 2016

Ground Rules

Purpose of this meeting:

- Discuss program objectives and structure.
- Provide opportunity for teaming prior to proposal deadline

Program not final until BAA published

- Please consult published BAA for final program specifics

Once BAA published and until the deadline for receipt of proposals

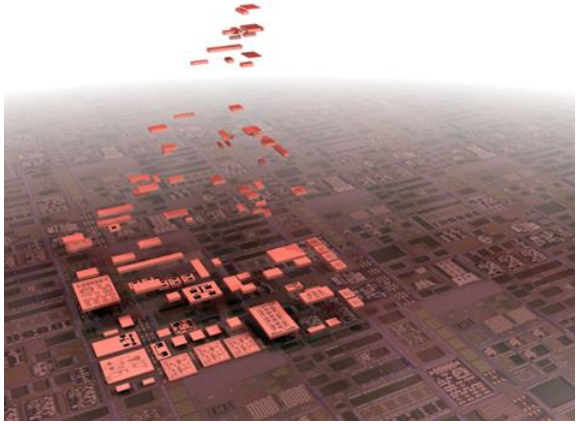
- Open communications between proposers and the program manager are encouraged.
- But: Information given to one proposer must be available to all proposers.
- The best way to get a question answered is to email it, and to retrieve your answer from the Questions and Answers list via the MTO solicitations website.
- Note that any question that contains distribution restrictions, such as 'company proprietary', will not be answered.

Questions:

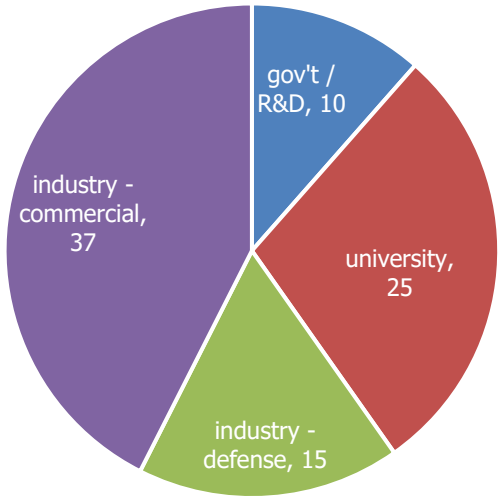
DARPA-BAA-16-62@darpa.mil

Welcome to the CHIPS Proposers Day

- 08:00-09:00: Registration
- 09:00-09:15: Bill Chappell - Opening Remarks
- 09:15-10:15: Dan Green - CHIPS Overview
- 10:15-10:30: Break
- 10:30-12:00: Presentations
  - 10:30-10:45: AMD - Bryan Black
  - 10:45-11:00: Adapteva - Andreas Olofsson
  - 11:00-11:15: GlobalFoundries - Ajit Dubey
  - 11:15-11:30: X-Celeprint - Chris Bower
  - 11:30-11:45: Northrop Grumman - Augusto Gutierrez-Aitken
  - 11:45-12:00: Summary - Dan Green
- 12:00-13:30: Lunch (self-organized)
- 13:30-15:30: Poster session and networking
- 15:30-16:00: Working with DARPA - Dan Green
- 16:00-16:30: BAA Q&A - Dan Green
- 16:30-17:00: Concluding Remarks - Dan Green



Organizations Participating Today



What is CHIPS?

CHIPS will develop **design tools, integration standards, and IP blocks** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic

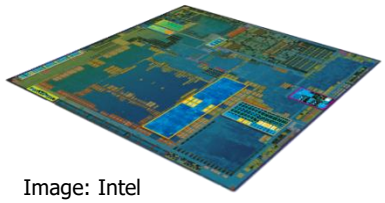
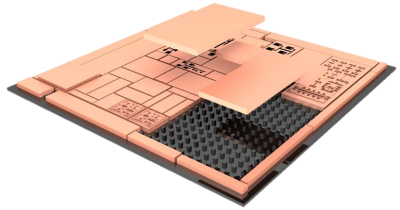
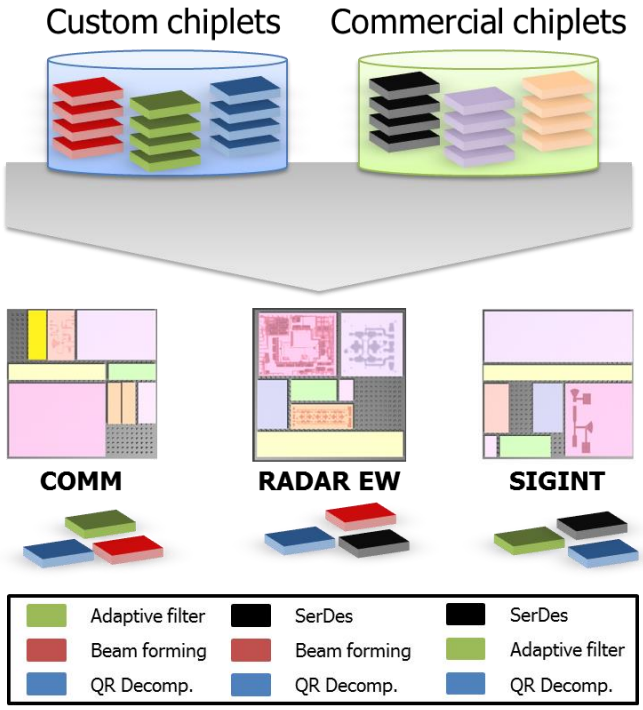


Image: Intel

Tomorrow – Modular

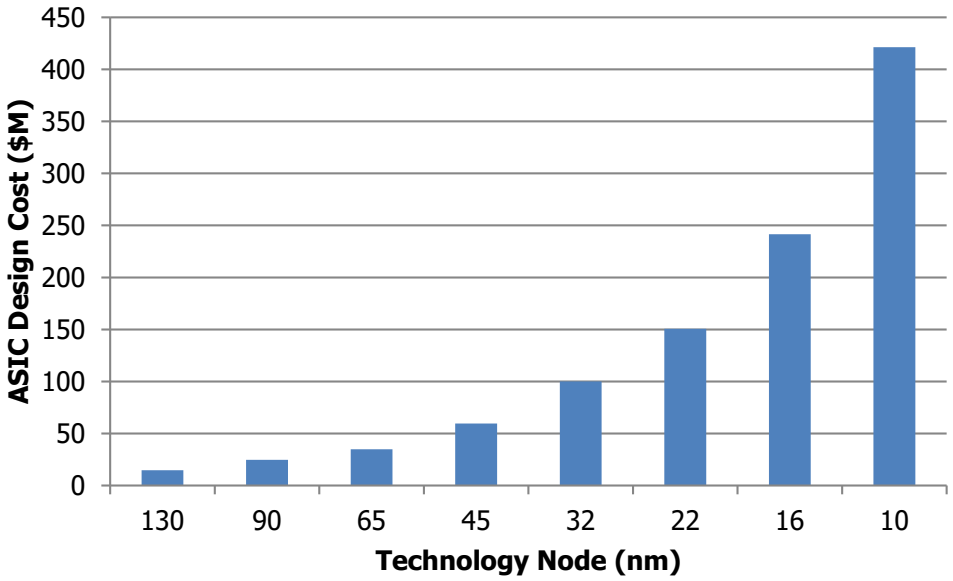


CHIPS enables rapid integration of functional blocks at the chiplet level



Why CHIPS? Advanced Si is Expensive…

Expensive to design at advanced nodes …



… which some commercial products can support …

© apple.com

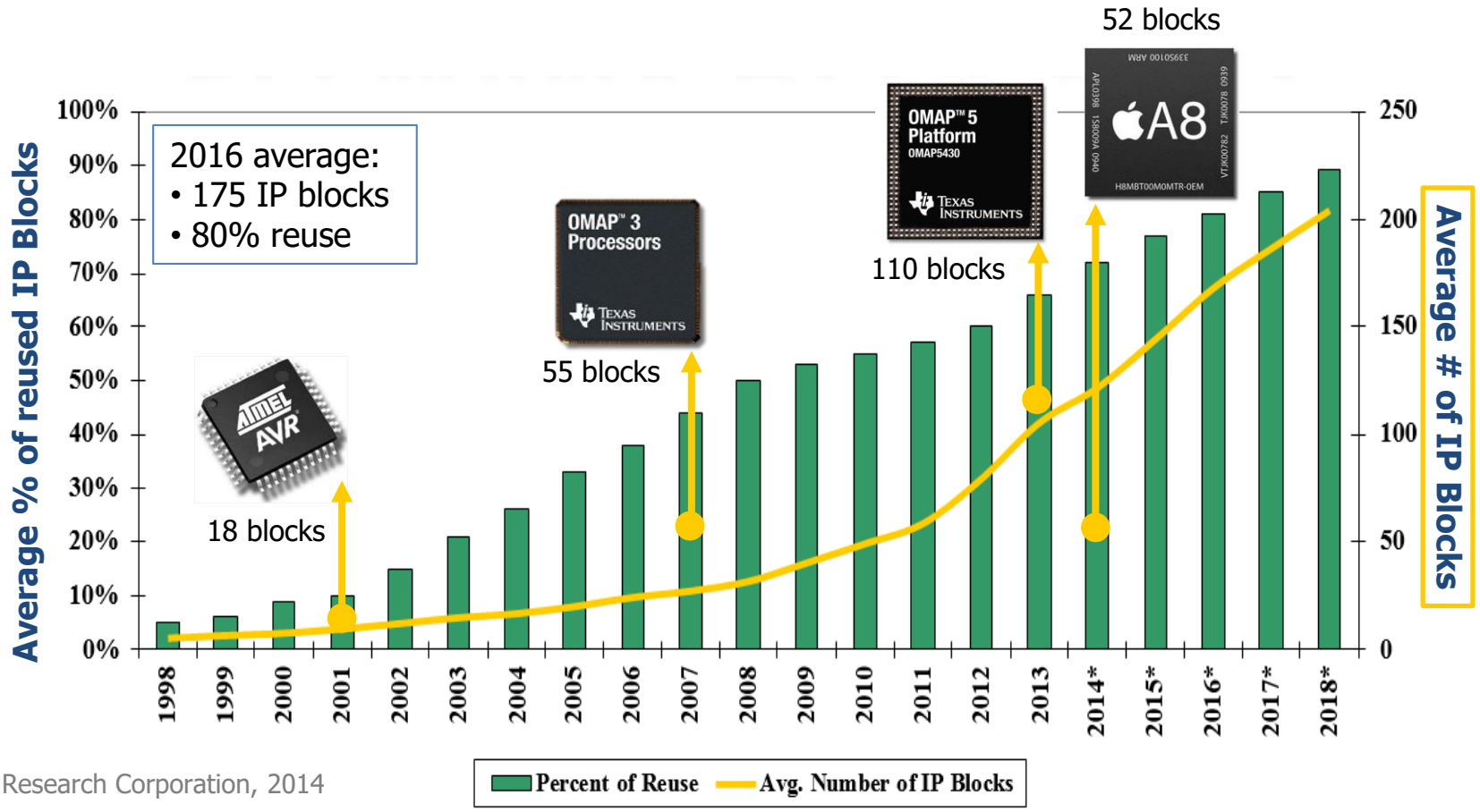
Fab cost for commercial electronics amortized over **one day's** worth of iPhones

… but DoD cannot.

Fab cost for a DoD IC amortized over **entire 29-year** acquisition of JSF

Source: "Cashing in with Chips" AlixPartners Semiconductor R&D outlook report, 2014.

…and IP Reuse is Common for Multicore SoCs…

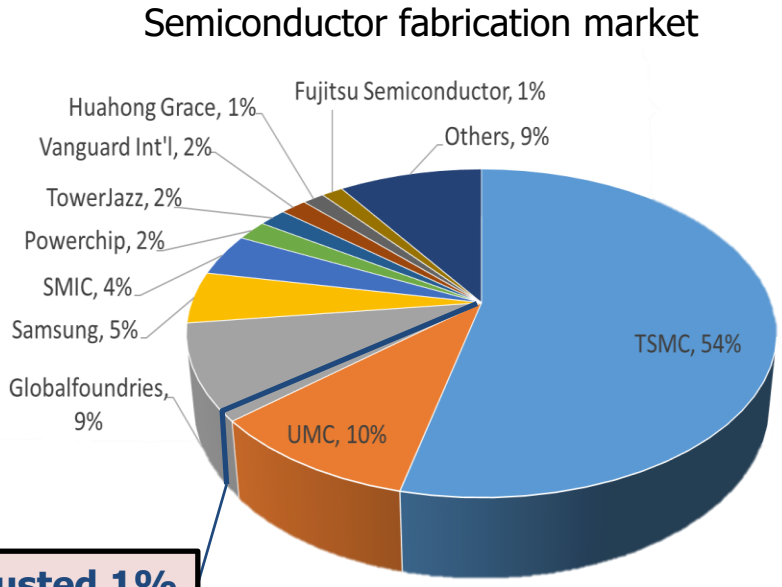


SEMICO Research Corporation, 2014

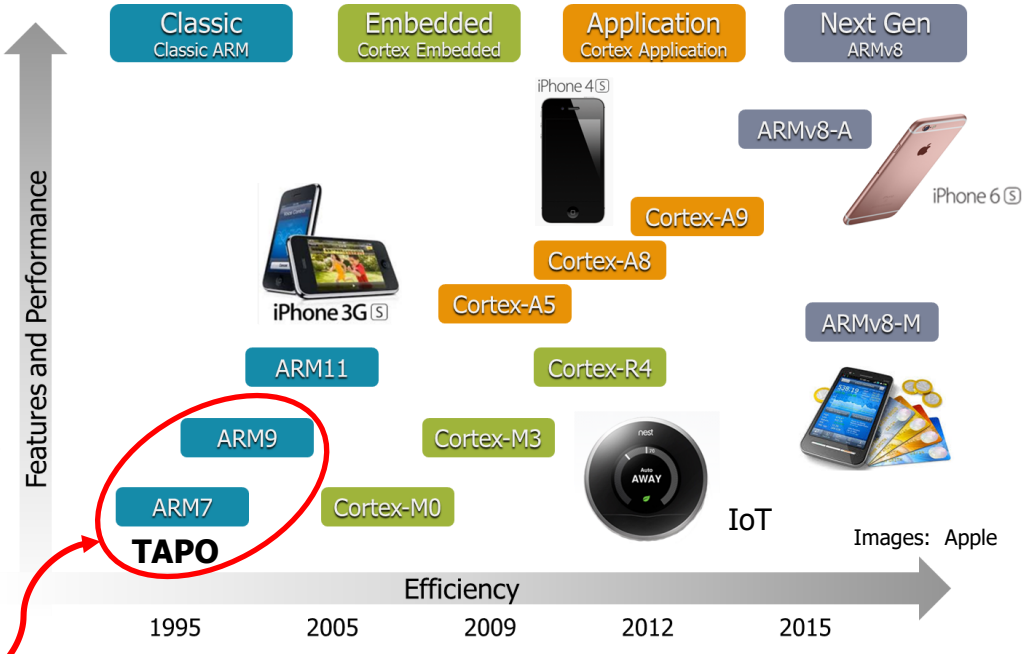
IP Reuse is increasingly important and shows no signs of slowing

…but Challenging for the DoD

Limited access to global pool of knowledge **and** talent



Trusted 1%

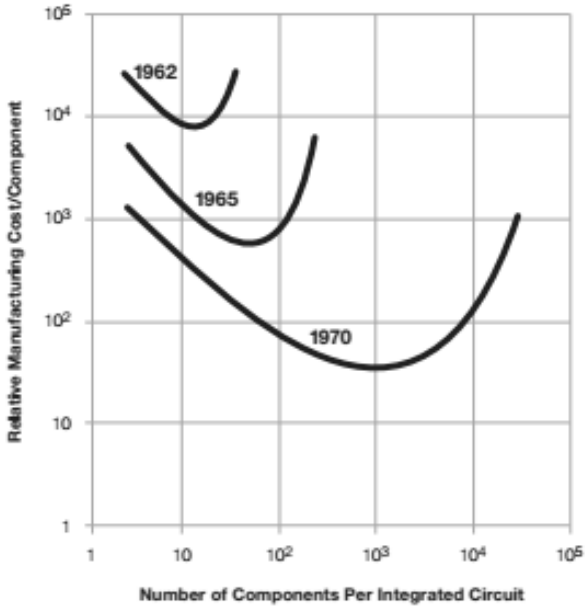


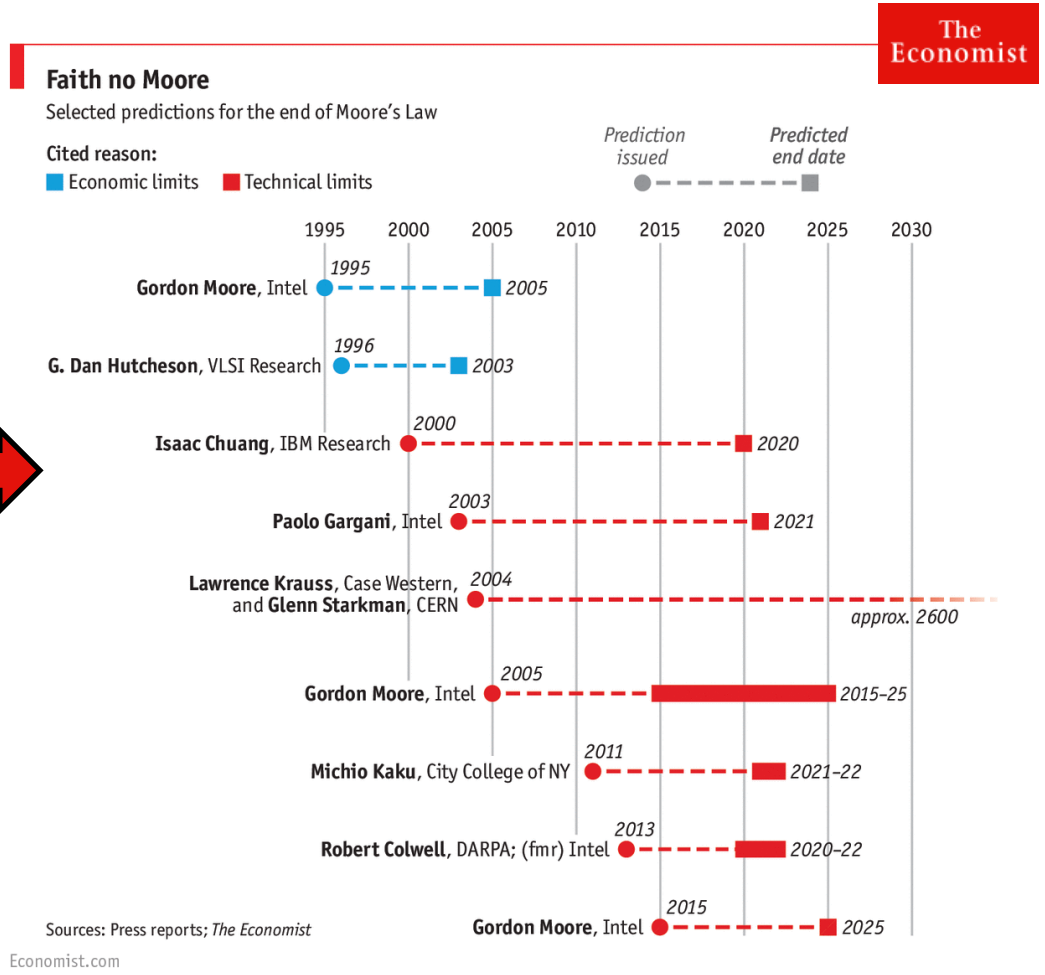
TAPO	TSMC
17 processes	>55 processes
>50 IP blocks	>8500 IP blocks

CHIPS is designed to expand the pool of IP and design resources

End of Moore's Law?

Moore's Law





End of Moore's Law means everyone is becoming low volume

Data source: Electronics Magazine, Economist.com

Moore's Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

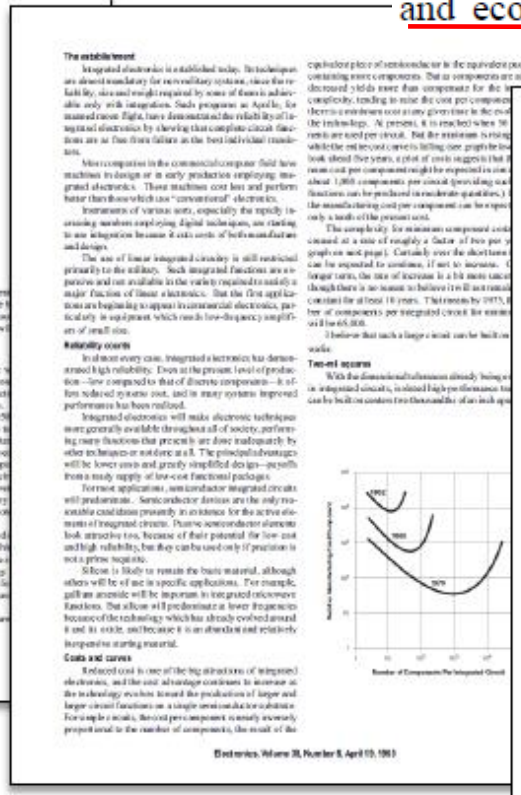
The experts look ahead

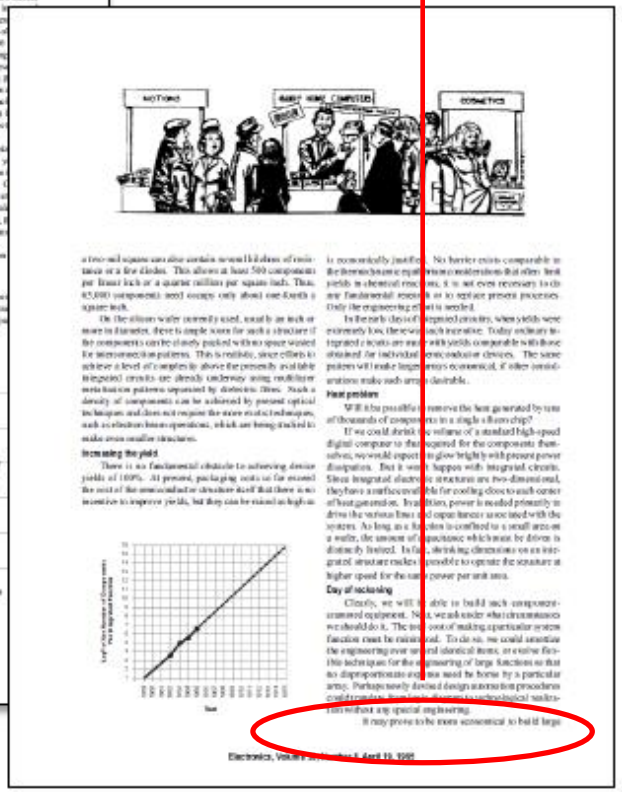
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.





G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

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Electronics, Volume 38, Number 8, April 19, 1965

More Than Moore?

⇨

More Of Moore

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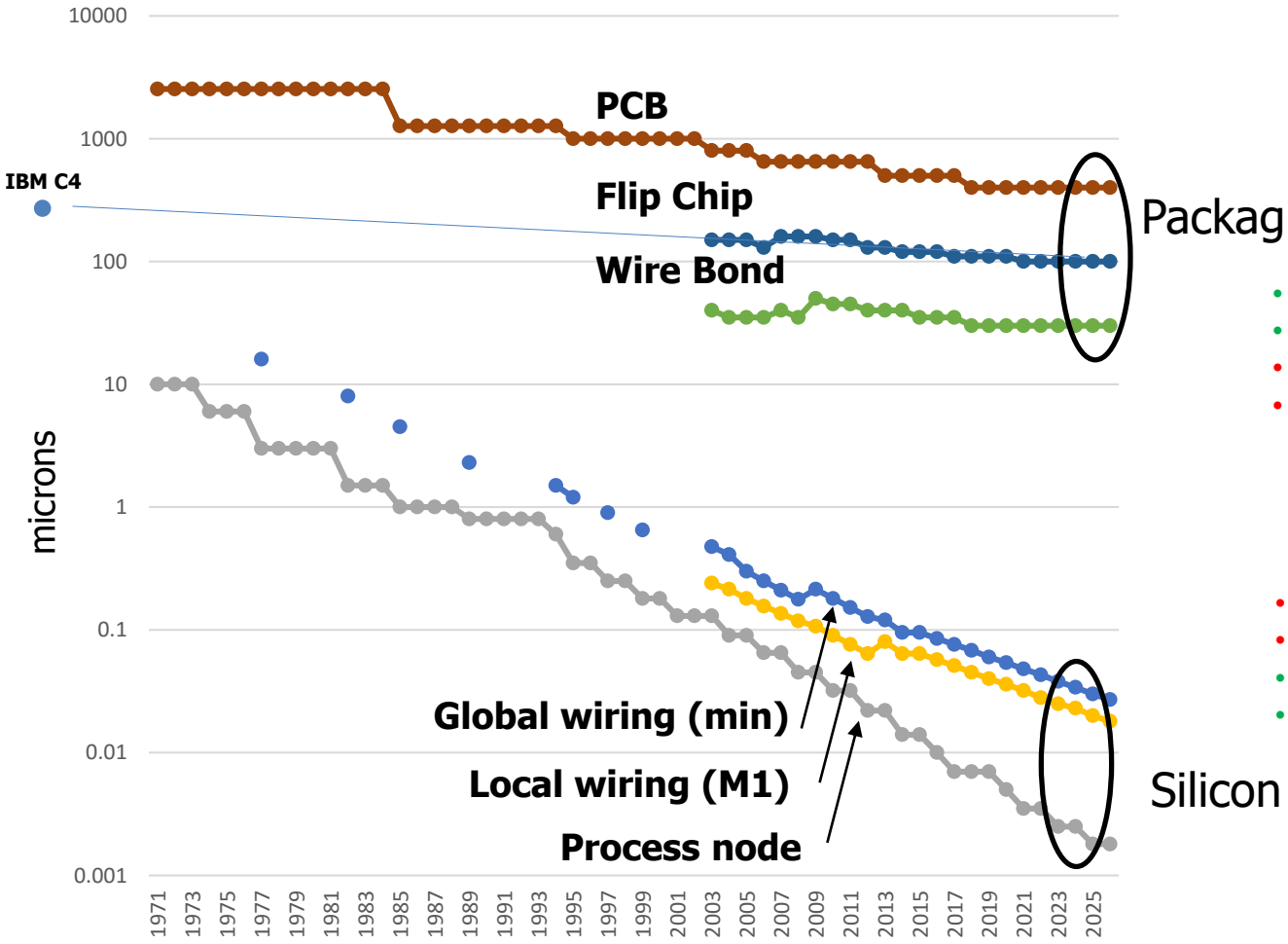
Conventional Assembly Has Attractive Features for HI … But Isn't Keeping Up on Pitch and Performance



Packaging

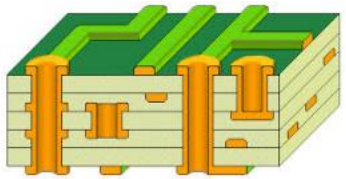


Image: EETimes

- Flexible heterogeneous integration
- Quick design / manufacturing turn
- Coarse pitch
- Lower performance

Silicon

- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

Image: IBM

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

Source: 2003-13 ITRS, Wikipedia

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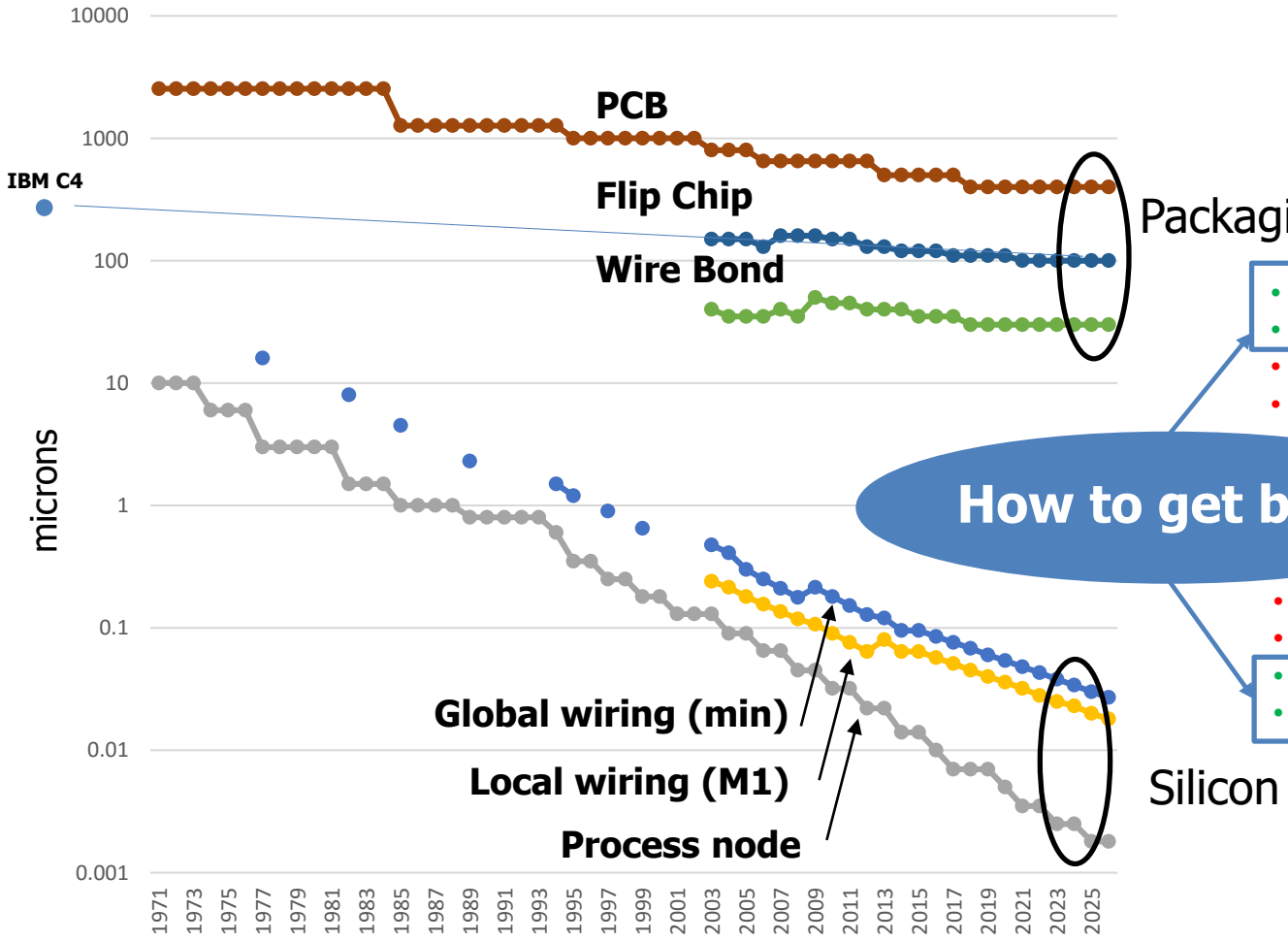

Packaging

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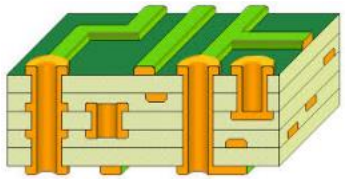

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- Flexible heterogeneous integration
- Quick design / manufacturing turn
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How to get both?

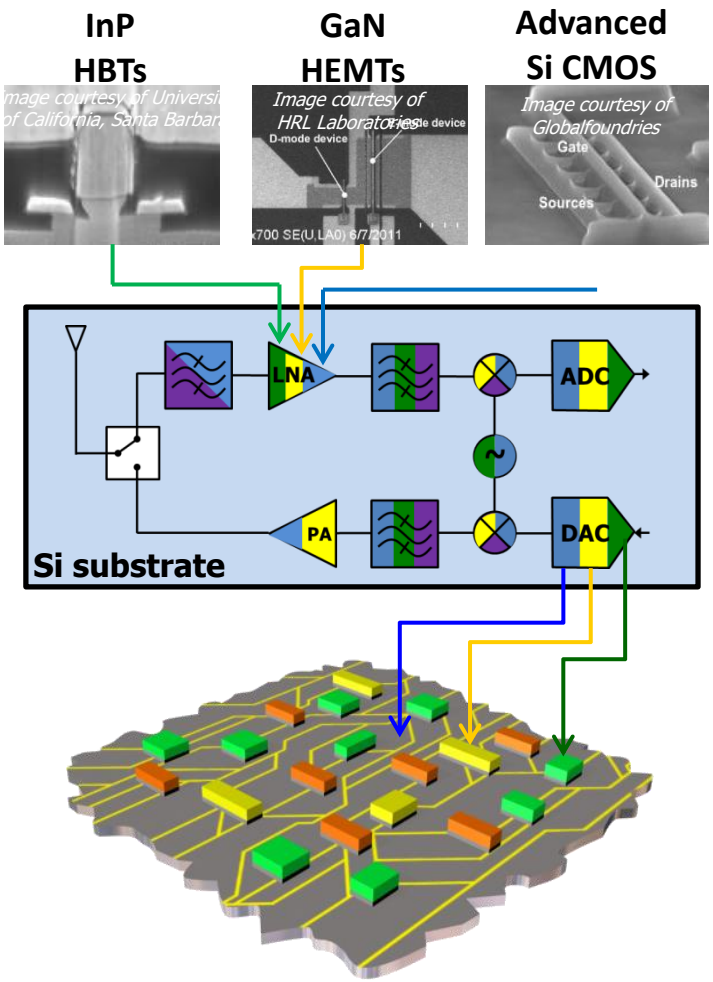
- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

Image: IBM

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

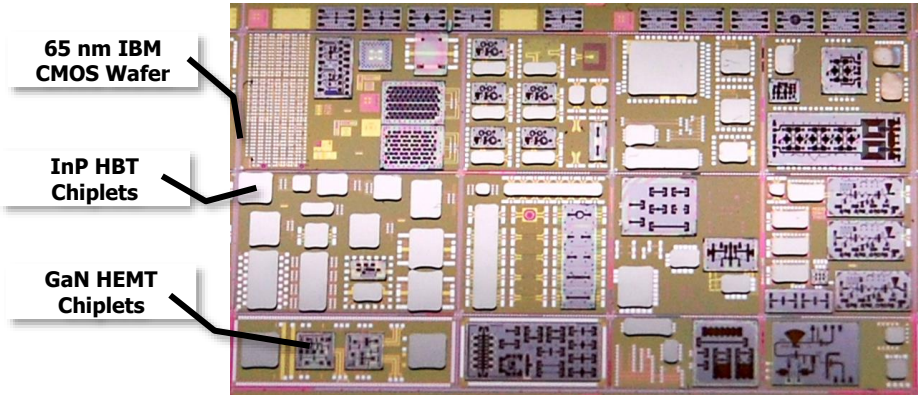
Source: 2003-13 ITRS, Wikipedia

Diverse Accessible Heterogeneous Integration (DAHI) Foundry for Heterogeneous Integration



Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

Heterogeneous technology integration in accessible foundry

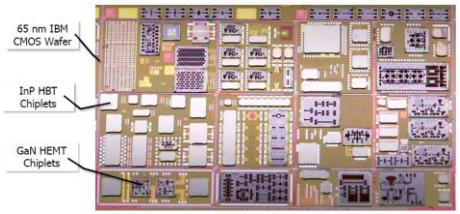


(first three-technology integration demonstrated in Jan 2015)

Image: Northrop Grumman

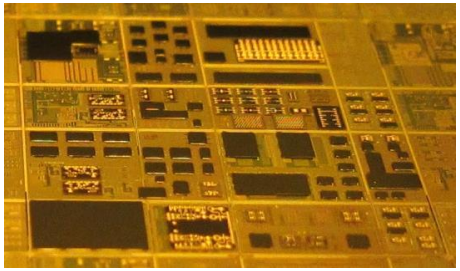
Goal: To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.

Heterogeneous Integration: Bridging the Gap



DAHI MPW0

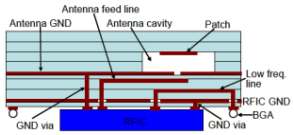
Images: Northrop Grumman



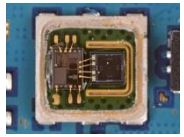
DAHI MPW1

Image: Prismark

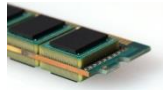
Package-based: Mature and flexible, but not scalable



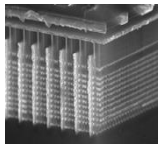
Advanced PCB



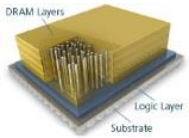
MEMS + ASIC
Image: ifixit



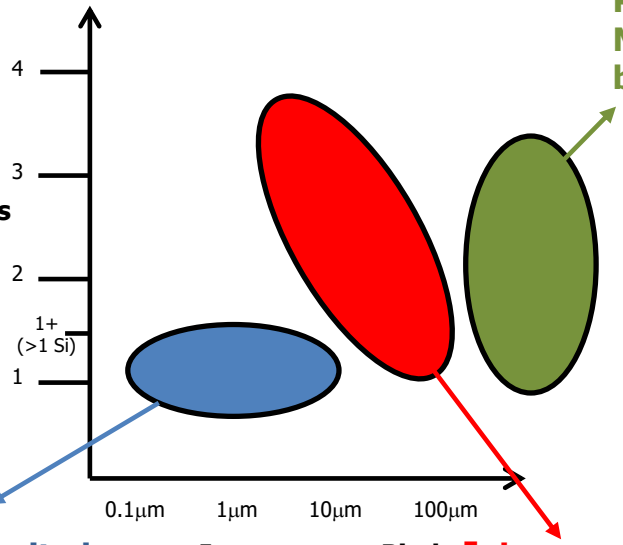
PoP memory
Image: Viking

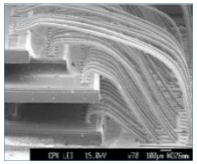


Monolithic 3D NAND
Image: Intel/Micron

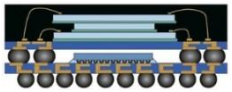


Processor + memory TSV
Image: Micron





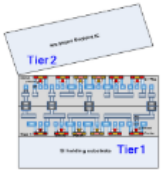
Stacked die (WB)
Image: Palomar



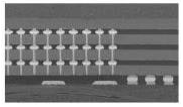
Processor + memory PoP
Image: Finetech

TSV / Wafer-scale: Immature or not well-suited for Heterogeneous Integration

Interposer-based: Scalable and flexible

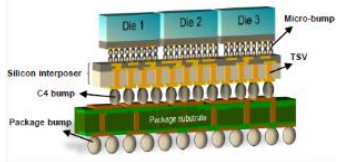


F2F wafer-bond
Image: Tezzaron



NAND/DRAM TSV
Image: Hynix

Image sensor TSV
Image: Sony

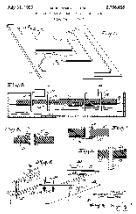


2.5D Si interposer
Image: TSMC

DAHI creates integration capabilities beyond current advanced interconnect technologies.

Propelled by **Standards** and **Modularity**: Electronics Industry Built via Integration on PCBs



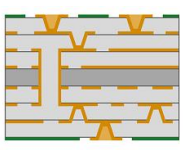
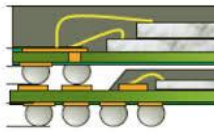




Image: Intel

"Printed circuit board" invented by Paul Eisler.

Early PCB demo in a radio.

First HVM PCBs enable proximity fuze during WWII.

Patent to US Army for PCB assembly.

IPC (Institute for Printed Circuits) founded; standards follow.

Multi-layer PCB invented.

Surface Mount Technology on PCBs revolutionizes manufacturing.

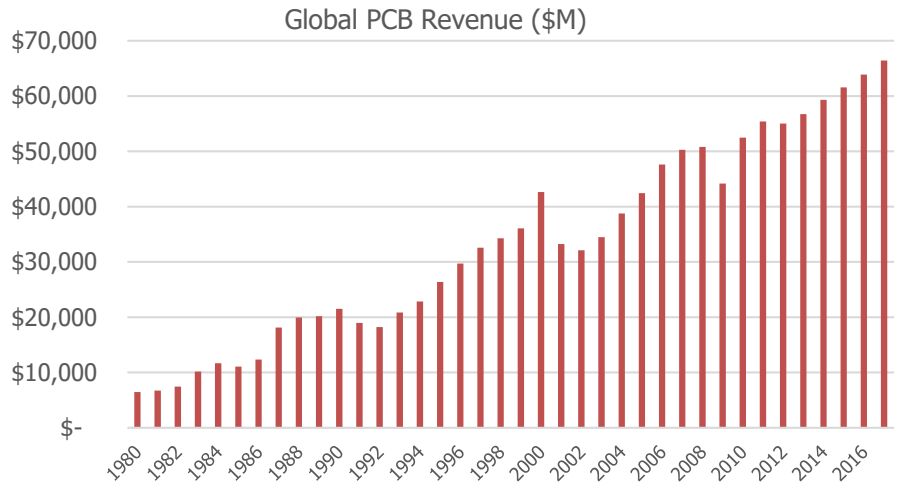
HDI / Microvia technology enables further integration.

First package-on-package standard from JEDEC

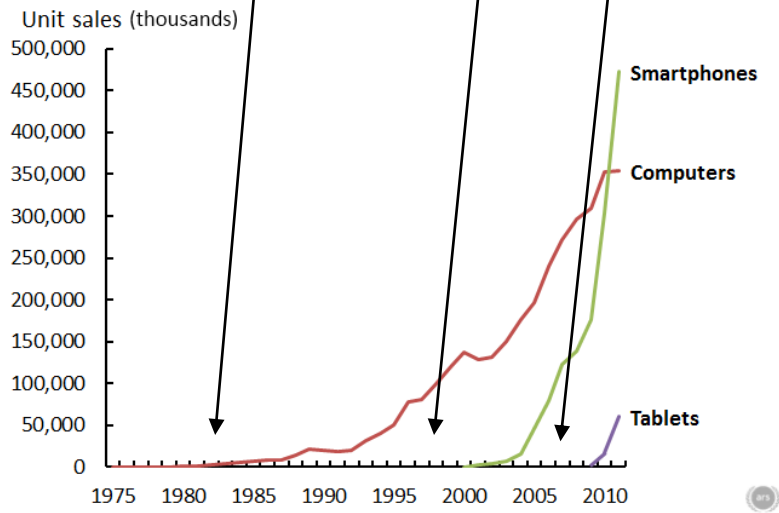
DoD jump-start

1936 1941 1943 1956 1957 1960 1980s 1995 2006

PCB industry sees steady expansion with DoD origins, standardization, and technology development.



Computers, smartphones, and tablet sales: 1975-2011

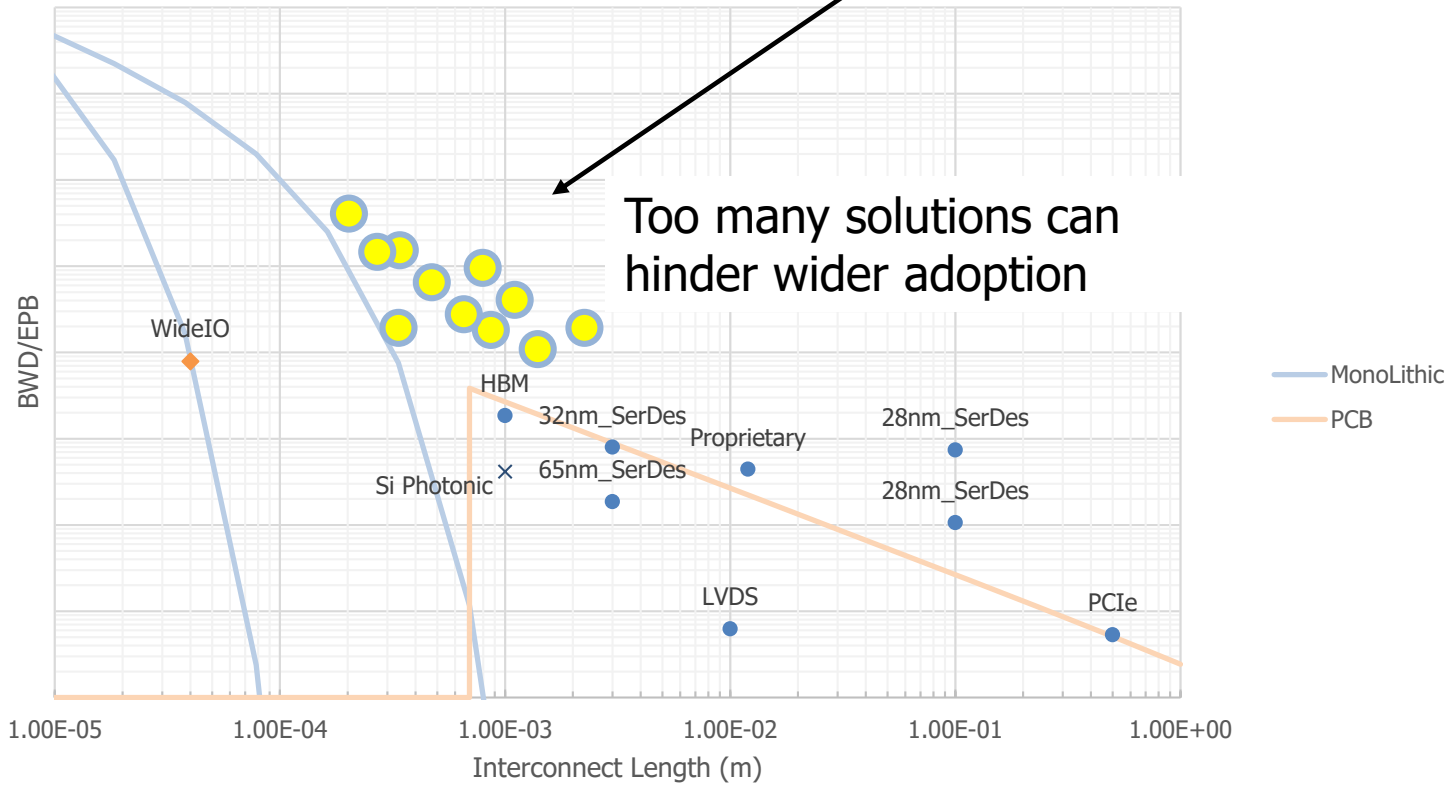


Sources: Prismark, Arstechnica, USPTO, Wikipedia, IPC, SMTA

Interface Standards: Too Many? Not Enough? How to Compare?

What standards will allow CHIPS to bridge the gap?

$$\frac{Gbps/mm}{Energy/bit}$$



CHIPS challenge: make a usable interface standard

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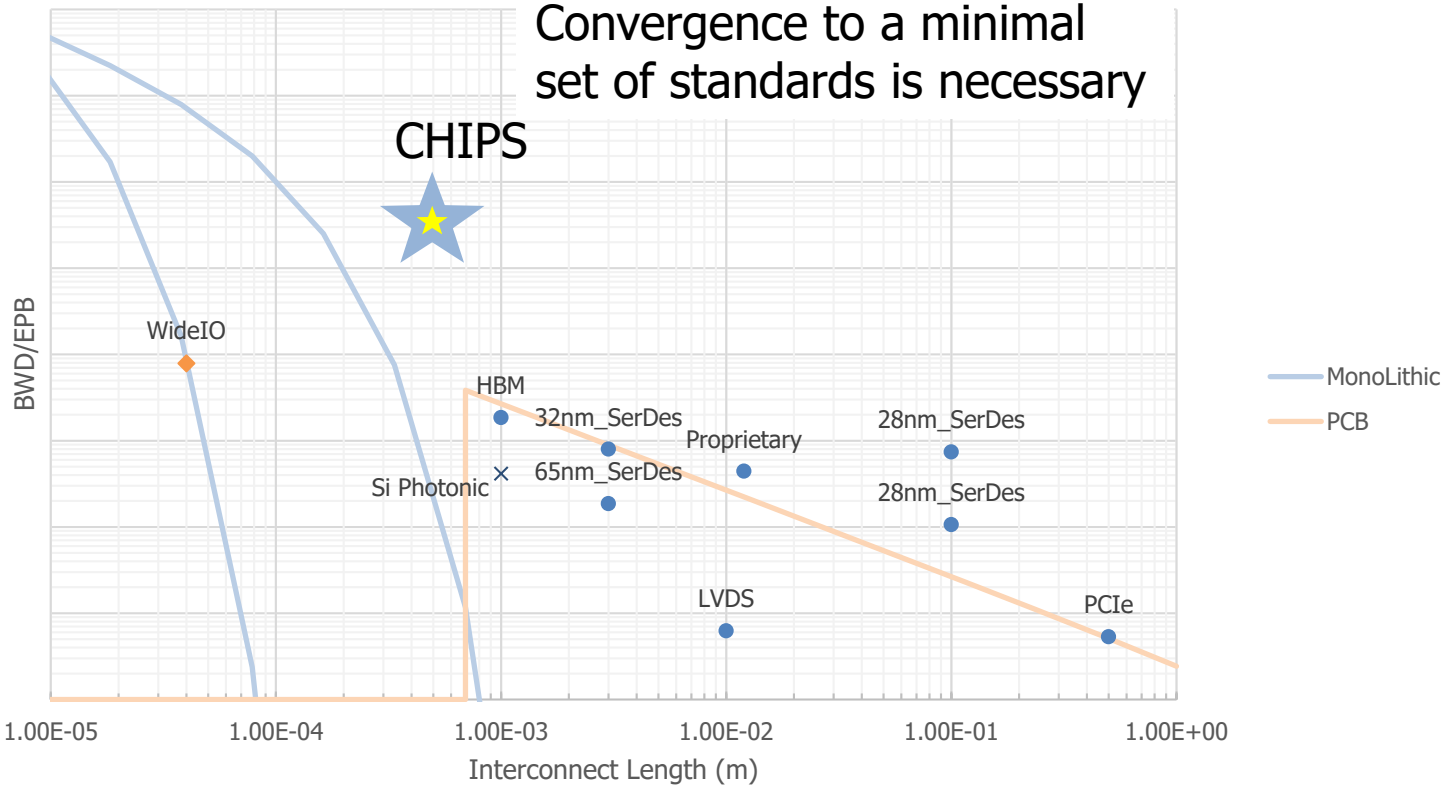

CHIPS challenge: make a usable interface standard

So what do we plan to do?

What is CHIPS?

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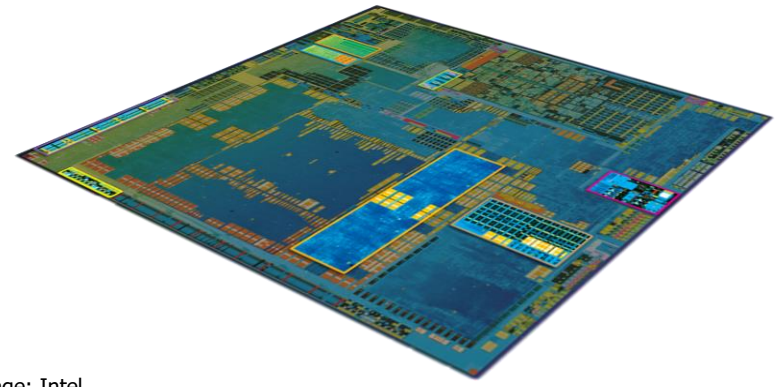
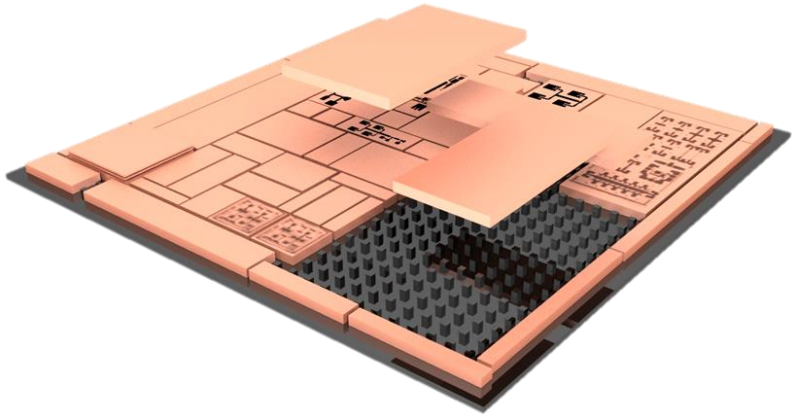


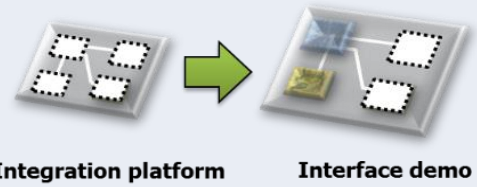
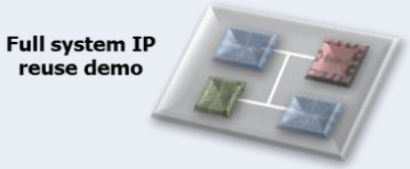
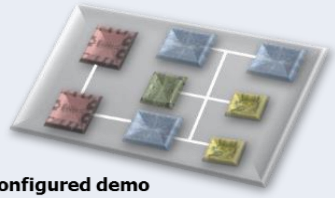
Image: Intel

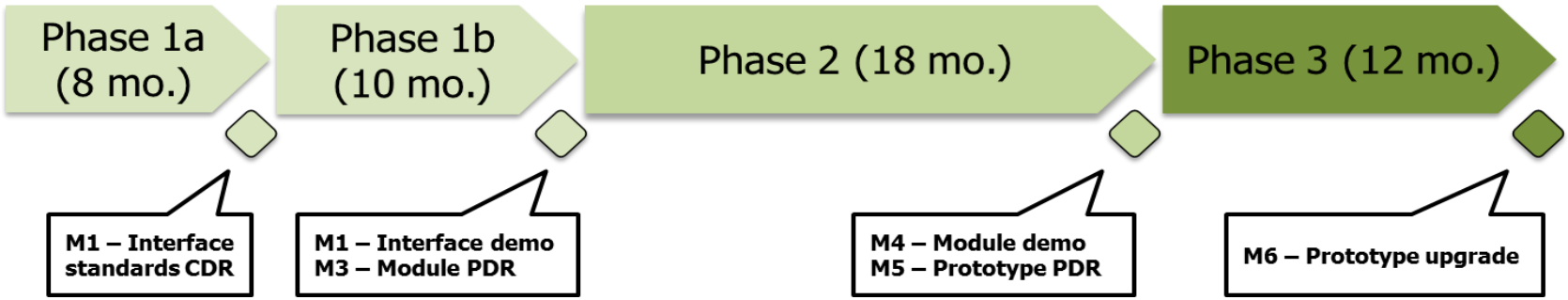
Tomorrow – Modular

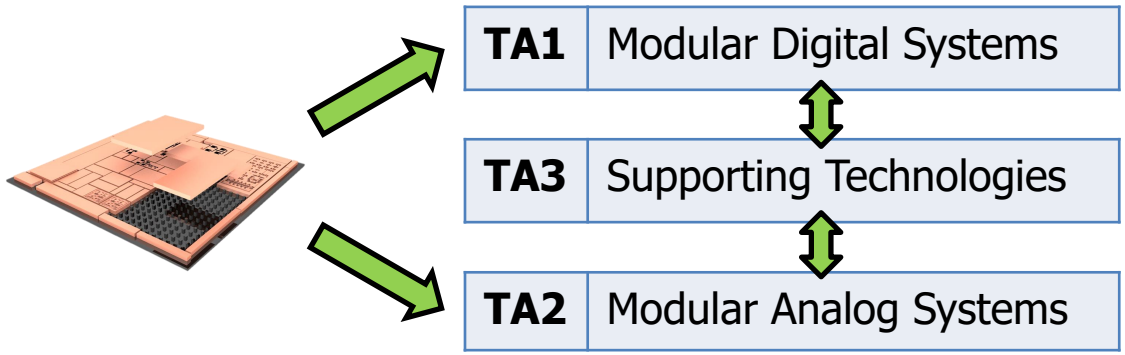


CHIPS is focused on creating modular IP – not new IP!

CHIPS Program – Structure and Timing

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	**Module Demo with IP Blocks**	**Rapid Module Upgrade**
		





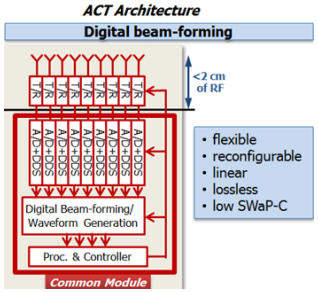
CHIPS Program - Metrics

CHIPS Program Metrics			
Metric	Phase 1	Phase 2	Phase 3
Design level			
IP reuse (1)	> 50% public IP blocks	> 50% public IP blocks	> 50% public IP blocks
Modular design (2)	—		> 80% reused, > 50% prefabricated IP
Access to IP (3)	> 2 sources of IP	> 2 sources of IP	> 3 sources of IP
Heterogeneous integration (4)	> 2 technologies	> 2 technologies	> 3 technologies
NRE reduction (5)	—	> 50%	>70%
Turnaround time reduction (5)	—	> 50%	>70%
Performance Benchmarks (performer defined)	—	>95% benchmark	>100% benchmark
Digital Interfaces			
Data rate (scalable) (6)	10 Gbps	10 Gbps	10 Gbps
Energy efficiency (7)	< 1 pJ/bit	< 1 pJ/bit	< 1 pJ/bit
Latency (7)	≤ 5 nsec	≤ 5 nsec	≤ 5 nsec
Bandwidth density	> 1000 Gbps/mm	> 1000 Gbps/mm	> 1000 Gbps/mm
Analog interfaces			
Insertion loss (across full bandwidth)	< 1 dB	< 1 dB	< 1 dB
Bandwidth	≥ 50 GHz	≥ 50 GHz	≥ 50 GHz
Power Handling	≥ 20 dBm	≥ 20 dBm	≥ 20 dBm

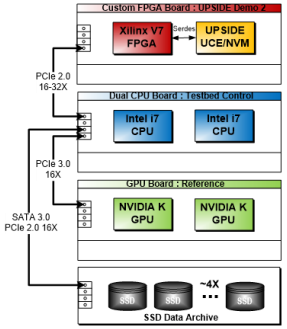
Notes:

1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
3. Valid sources of IP must be those that are outside of the performer team.
4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
7. Performance relating to transferring data between chiplets compared against a benchmark design.

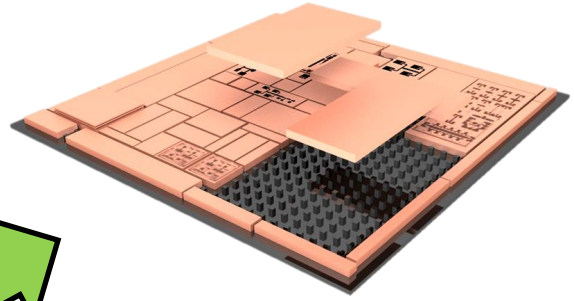
TA1: Modular Digital Systems



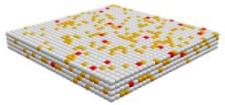
Arrays at Commercial Timescales (ACT)



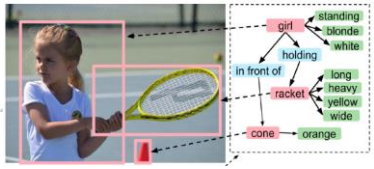
Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE)



"Modularization"



Intelligent Computing Algorithm Development



Cortical Processor

Semiconductor Technology Advanced Research Network (STARnet)

Targets modular circuits that leverage digital interfaces.

Looking for designs that:
- Leverage modular interface
- Reuse existing IP
- Are DoD relevant

Includes:
- Analog/Mixed signal circuits with digital interface
- non-DARPA designs

Others: CLASS, Mobile Hotspots, MFRF, ViSAR, ELASTx, …

Don't need to start from scratch!

TA2: Modular Analog Systems

RF Unit Cell

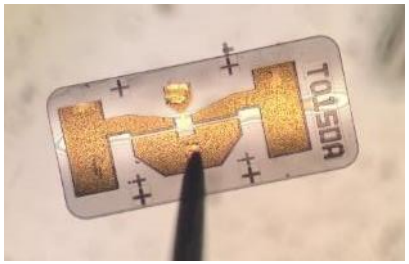
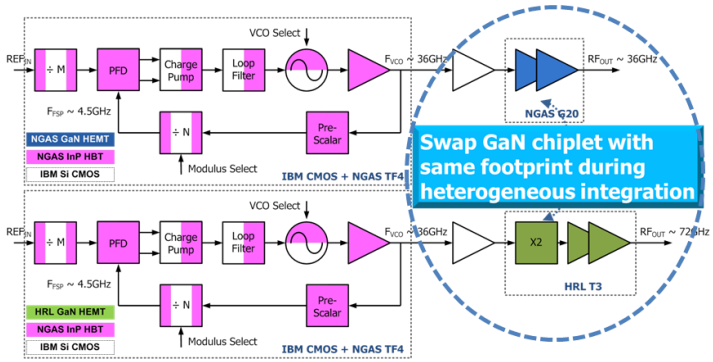
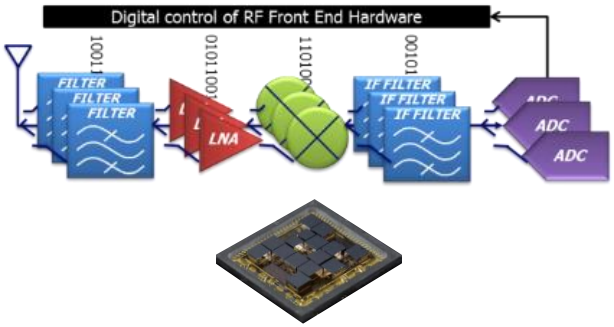


Image: NRL

Modular Devices



Modular Signal Blocks



Range of analog building block granularity

Seeks to realize modular pseudolithic microwave integrated circuits:

- Leverage modular building blocks
- Demonstrate performance into mm-Wave regime
- Develop sustainable attractive business models

Balance granularity with accessibility, reusability and cycle time

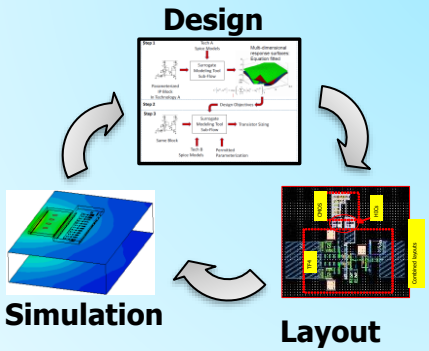
TA3: CHIPS Supporting Technologies

- Design tools
  - Heterogeneous integration
  - Modular design flows
- Assembly methods
  - Fine pitch
  - Small device handling / testing
  - Multi-device technology processing
- IP blocks

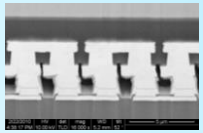
Sample Digital IP

Processor	Interface	Memory
Image signal	SerDes	Controller
Audio signal	USB	DRAM
Digital signal	PCIe	SRAM
Compression		Flash
GPU		
CPU		
Machine Learning		

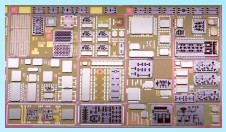
Design Tools



Assembly Methods



Fine pitch interconnects



Heterogeneous integration

Images: Northrop Grumman

Sample Analog IP

Amplifiers	Passives
LNA	Filters
DAC / ADC	PMIC
Envelope Tracker	Transistor Unit Cell
Mixer	PLL

Key challenge will be alignment to TA1 and TA2

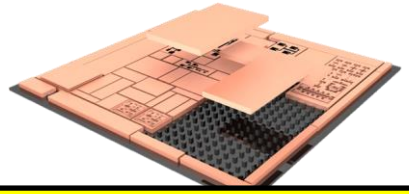
Non-CHIPS Developments

Technology NOT germane to CHIPS:

- New device technologies
- Wholly new circuits
- Security specific processes (e.g. obscuration, split fabrication)

Focus is on making modularity work!

CHIPS end state vs. conventional supply chain

	IP Blocks	CAD tools	Architecture	Design	Verification	Fabrication	Pkg / Test	Systems
Commercial	ARM TSMC Cadence Imagination	Cadence Mentor Graphics Synopsys	Google Apple Microsoft Samsung	Qualcomm Broadcom Apple TI Marvell	Qualcomm Broadcom Apple TI Marvell	TSMC SMIC GlobalFoun. Intel Samsung	TSMC ASE Group Amkor	Google Apple Microsoft Samsung
DoD	ARM Global Foundries	Cadence Mentor Graphics Synopsys	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Northrop TowerJazz HRL Global Foundries	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE
CHIPS	ARM TSMC Cadence Imagination Raytheon Northrop Lockheed Boeing BAE	Cadence Mentor Graphics Synopsys	Raytheon Northrop Lockheed Boeing BAE	 CHIPS		Northrop Novati US OSAT		Raytheon Northrop Lockheed Boeing BAE

Design specs

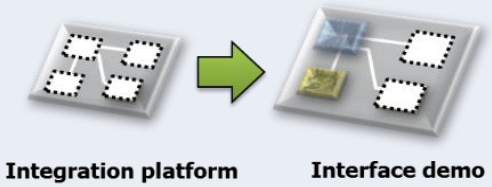
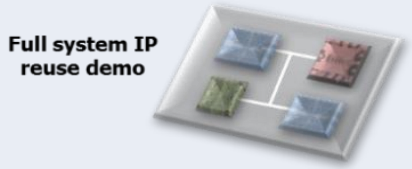
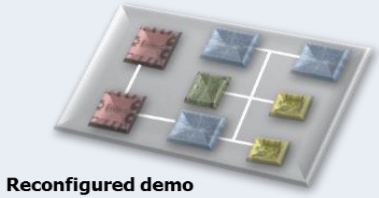
Chiplets

Commercial	Defense	Emerging	Distributor
TSMC Intel Global Foundries	Northrop Raytheon HRL	Jariet ? Intrinsix Flexlogix	Mouser ? Digi-Key

(Note: Companies listed are examples only.)

Trusted sources for critical components

CHIPS Program – Program Summary

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	**Module Demo with IP Blocks**	**Rapid Module Upgrade**
		

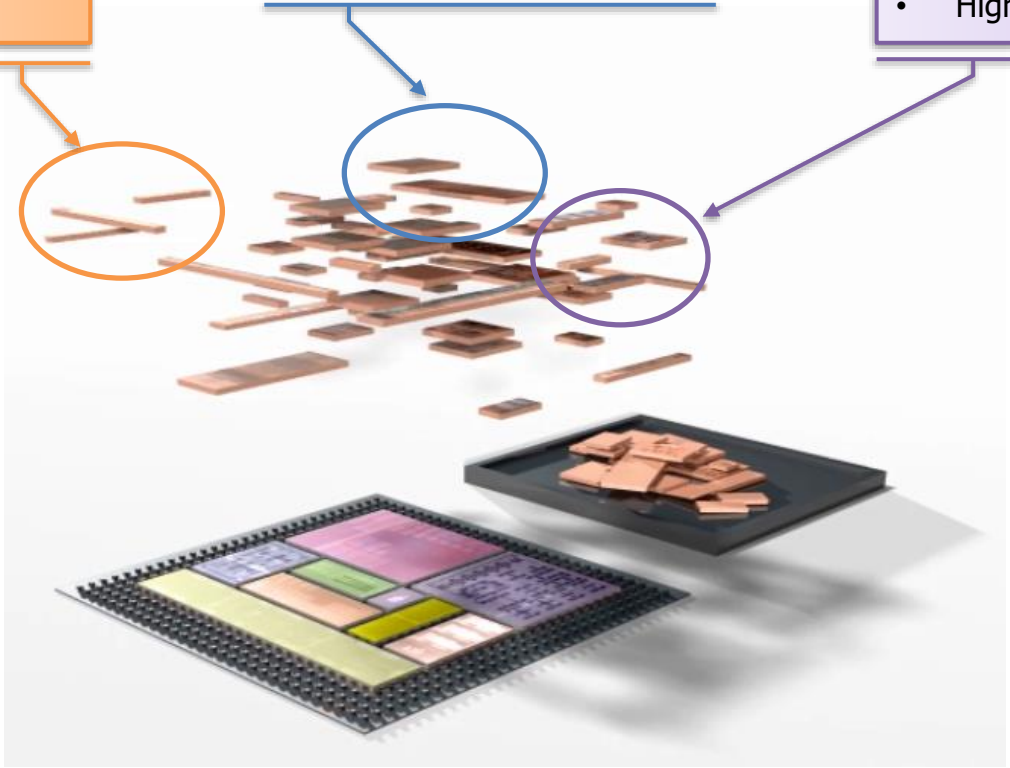
TA1 Modular Digital Systems		
• Modularize existing digital design via interface standard. • Critical design review for standards at 8-month mark. • Demonstrate functional IP blocks.	• Demonstrate functional digital design. • Cost + design cycle analysis. • Present design for Phase3.	• Demonstrate rapid upgradability. • Cost + design cycle analysis comparing CHIPS module versus a monolithic implementation.
TA2 Modular Analog Systems		
• Modularize existing analog design via interface standard. • Review design and interface at the 8-month mark. • Demonstrate interconnect performance.	• Integrate blocks into PLIC. • Analyze against SoA for performance, unit cost, NRE, and turnaround time. • Develop business model for modular analog ecosystem.	• Demonstrate rapid assembly of new PLICs. • Analyze against SoA for performance, unit cost, NRE, and turnaround time. • Cost / development time analysis of CHIPS PLIC vs MMIC.
TA3 Supporting Technologies		
• Design Tools, Assembly Methods, IP in support of TA1 and/or TA2 tasks and metrics		

What CHIPS Means for the DOD

Reusable function blocks
- QR decomposition
- Waveforms
- FFT

Access to Commercial IP
- Memory
- SerDes
- Processors

Big Data Movement
- Image processing
- Machine Learning
- High-speed chiplet networks



CHIPS modularity targets the enabling of a wide range of custom solutions

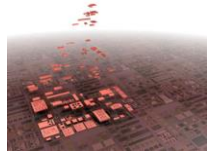
What do we plan to spend? and When?

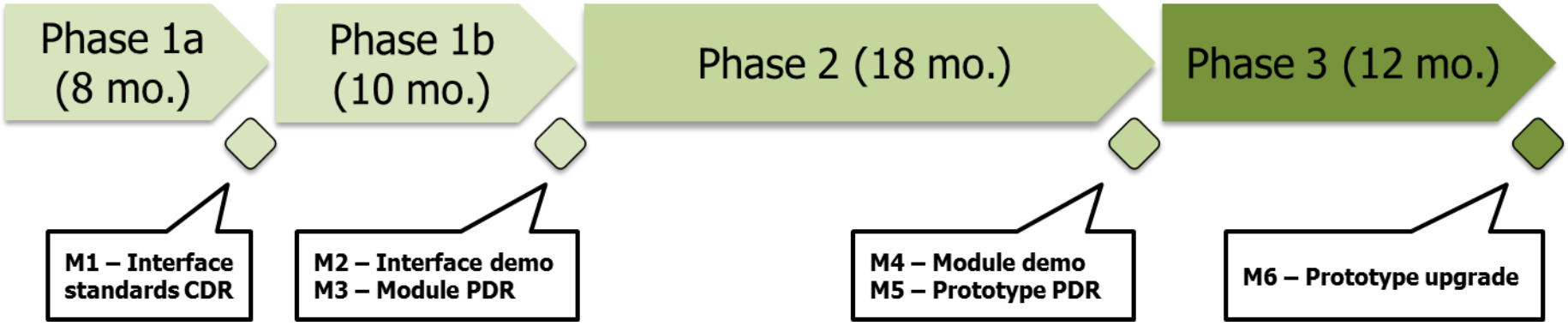
- **Anticipated Funding Available for Award:** DARPA anticipates a funding level of approximately $70M for the CHIPS program.
- **Anticipated individual awards** – Multiple awards in each Technical Area are anticipated.
- **Anticipated funding type** - 6.2 and/or 6.3
- **Types of instruments that may be awarded** – Procurement contract, grant, cooperative agreement or other transaction.

Important Dates	
Proposers Day	21-Sep-2016
BAA Release (est.)	26-Sep-2016
Abstracts Due*	26-Oct-2016
FAQ Deadline*	23-Nov-2016
Proposals Due*	7-Dec-2016
Program Kick-Off*	Mar-2017

*Dates are a function of actual BAA release date.

CHIPS Summary





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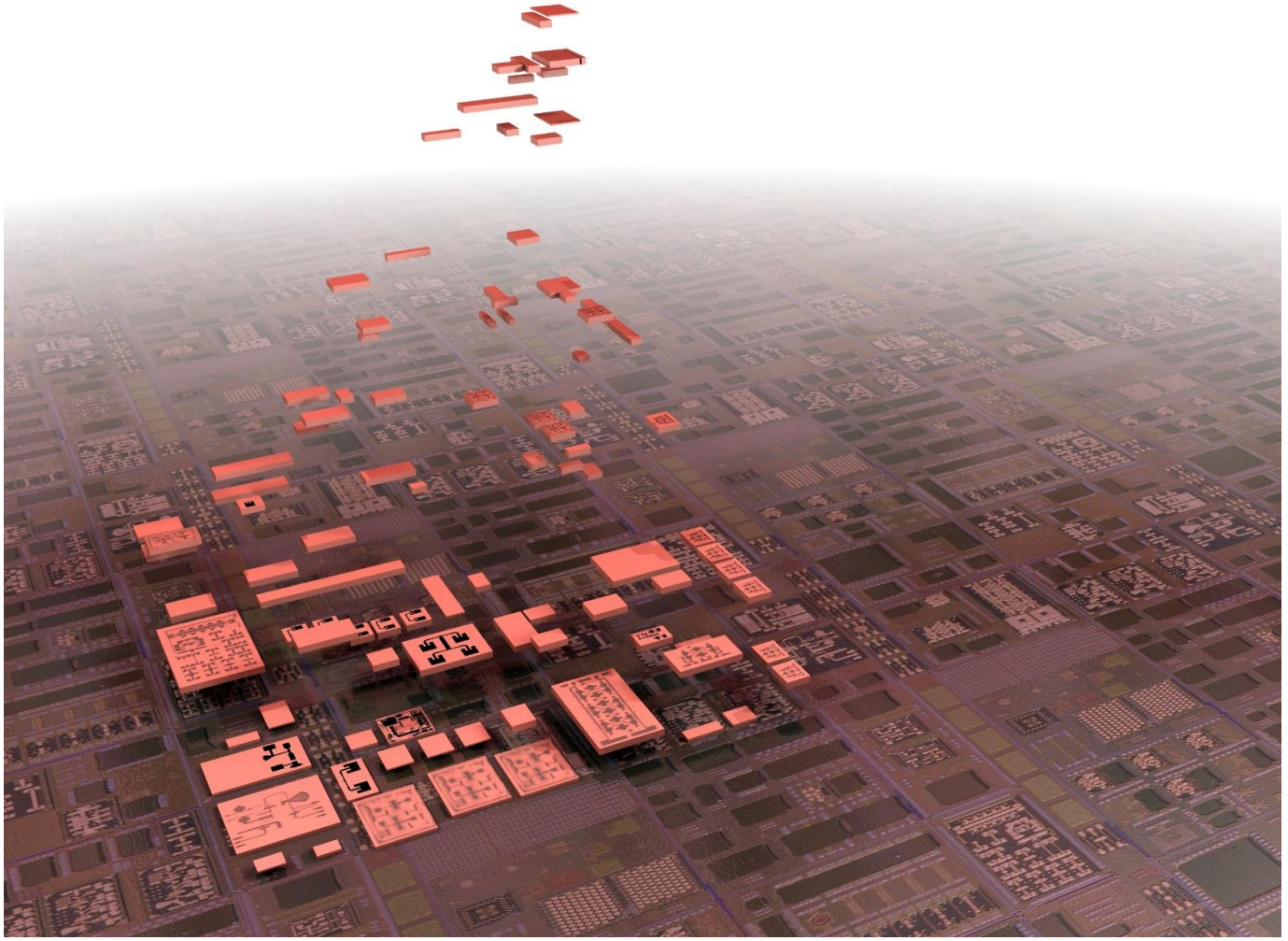
TA1	Modular Digital Systems
TA2	Modular Analog Systems
TA3	Supporting Technologies

Questions: DARPA-BAA-16-62@darpa.mil

CHIPS future of heterogeneous integration



Requires a lot of pieces coming together!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